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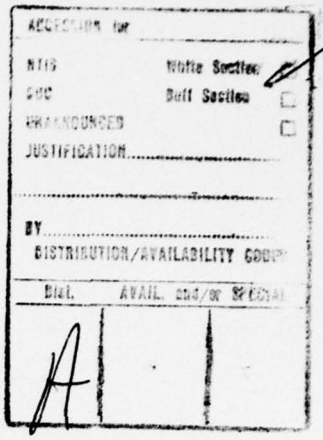

EFFICIENCY OF COMPACT TESTING FOR SEQUENTIAL CIRCUITS

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ABSTRACT

Compact testing uses random inputs to test digital circuits. Detection is achieved by comparison between some statistic property of the circuit under test, like the frequency of ones on the output line, and the same property for the fault-free circuit. In this paper we show that compact testing can be efficiently used for sequential machines, although it has some inherent limitations. Synchronization is achieved by a long sequence of random inputs whose length is circuit dependent. However, for most sequential circuits synchronization can be achieved in a few seconds. The great majority of failures inside the memory elements are easily detected, even with short tests. Compact testing also detects most of the failures in the combinational parts. There, its efficiency is largely dependent upon the test length and also the characteristics of the random number generators. However, even the most subtle failures may be detected if the test has sufficient length. Some of the requirements and trade-offs to achieve efficient detection are presented.

Index Terms: Sequential circuits, testing, random inputs, synchronization, failures, detection.

I. INTRODUCTION

The ever increasing complexity of digital circuits has made the testing problem extremely difficult. The deterministic methods for test generation (D. Algorithm, [J.P. Roth, 1967], [W.G. Bouricius, 1971]; Boolean Difference, [F.F. Sellers, 1968]; Poage's Method, [J.P. Poage, 1964]; etc.) become prohibitively expensive for large circuits. The number of stuck-at faults increases exponentially with the number of gates. For large LSI chips, like microprocessors, the amount of computation required to generate a vector test set that covers all single stuck-at and some multiple faults is extremely large. Furthermore, LSI failure modes may not conform to the stuck-at model and such failures as pattern-sensitive failures may not be covered by the test obtained.

Random test generation methods [M.A. Breuer, 1971], [J.C. Rault, 1971], [V.D. Agrawal, 1972] and [P. Agrawal, 1975] are used to overcome some of the computation costs of the deterministic methods. Random input patterns are fed to a prototype of the circuit to test (or a simulator) and are analysed for their ability to catch failures. These methods give, in general, far larger test sets. However, there have been some studies to try to optimize them (by assigning different weights to the input leads [M.D. Schnwinmann, 1975] or by interactive use [K.P. Parker, 1976]).

Some testing methods bypass the need for any prior test generation. Quite often, testing is economically achieved by comparing the outputs of the unit under test with the outputs of a known good unit (also called "gold unit") while both units are fed by the same sequence of random inputs. The efficiency of such testing methods has been analysed by

[J.J. Shedlestky, 1975]. However, the need for a gold unit may be bothersome (large or expensive gold unit). Moreover, the reliability of the gold unit is not guaranteed and the synchronization of the two units may also cause problems.

Recently, a new testing method, which also does not necessitate prior test set generation, has been implemented in some test equipments. The unit under test is fed by random or pseudo-random inputs, and some statistics of the outputs (for example, the number of logic ones or transitions) are computed. If the output statistics satisfy some known properties (for example, a given frequency of ones), the unit is said to have passed the test. We will refer to such testing methods as compact testing. An example of commercial testers implementing this method is the Fluke Trendar 1000 Logictester. Such a method has been investigated by [J.P. Hayes, 1975], [J.P. Hayes, 1976] and [K.P. Parker, 1976]. Its general efficiency, when applied to combinational circuits, has been investigated by [J. Losq, 1976]. The goal of this paper is to obtain quantitative measures for the efficiency of compact testing applied to sequential circuits.

II. TEST DESCRIPTION

Compact testing of sequential circuits is achieved in three steps. The first part of the experiment consists in feeding the circuit a long sequence of random inputs. The rationale for this is to try to synchronize the circuit. The next step consists in sending another long sequence of random inputs during which output statistics are gathered. The third step is the comparison between the obtained statistics and the correct ones. The circuit is then declared fault-free if the statistics match. For this study, one will assume that the output statistics that are gathered during the second step of the experiment are the frequencies of logic ones on each output line. The study by [J.P. Hayes, 1976] tends to conclude that it is the best statistic. Figure 1 gives the general description of compact testing.

The length of the input sequence during the first step of the experiment (the synchronization step) will be denoted by T_0. Similarly, the length of the sequence during the statistic gathering step will be denoted by T.

The circuit under test is a sequential machine, M, characterized by its five t-uple [E.J. McCluskey, 1965], [M.A. Arbid, 1969]:

$$M = \langle I, O, Q, \delta, \lambda \rangle$$

with I = input alphabet,

O = output alphabet,

Q = state set,

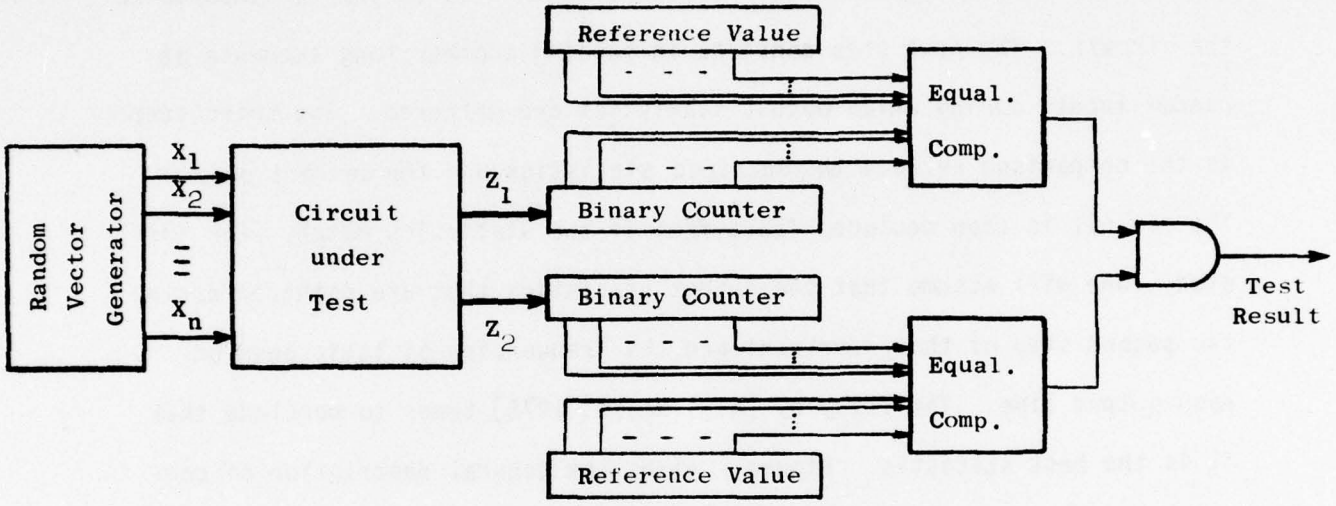


Fig. 1. General conception of random testers for n-input 2-output circuits.

$\delta = Q \times I \xrightarrow{\delta} Q$ = state transition function,

$\lambda = Q \times I \xrightarrow{\lambda} O$ = output function in Mealy-type machines,

$Q \xrightarrow{\lambda} O$ = output function in Moore-type machines.

In the following we will adopt the following conventions:

- The machine has n binary input variables: $X_1, X_2, \ldots, X_n$,
- All the 2^n possible input vectors, $A_0, A_1, \ldots, A_{2^n-1}$ accepted by the machine,
- The machine has m binary output variables, $Z_1, Z_2, \ldots, Z_m$,
- The 2^m output vectors are denoted by $B_0, B_1, \ldots, B_{2^m-1}$
- The machine, when it is fault free, has q states, $Q_1, Q_2, \ldots, Q_q$,
- The machine is a Mealy-type machine (Moore-type machines are special case of Mealy-type machines).

Mathematically, one has the following relations:

$$M = \langle I, O, Q, \delta, \lambda \rangle ,$$

$$I = X_1 \times X_2 \times \cdots \times X_n = \left\{ A_0, A_1, \ldots, A_{2^n-1} \right\} ,$$

$$O = Z_1 \times Z_2 \times \cdots \times Z_m = \left\{ B_0, B_1, \ldots, B_{2^m-1} \right\} ,$$

$$Q = \left\{ Q_1, Q_2, \ldots, Q_q \right\} ,$$

$$X_1, X_2, \ldots, X_n, Z_1, Z_2, \ldots, Z_m = \{0,1\} ,$$

A_i corresponds to the input vector for which $\langle X_1, X_2, \ldots, X_n \rangle$ is the binary representation of i.

The random vector generator that drives the circuit under test (cf. Figure 1) produces random inputs. It is stationary and characterized by the probabilities, x_i, that the logic value on line X_i is a one. So, one can easily obtain the set of probabilities, a_i's, of all possible input vectors, [K.P. Parker, 1976]. For clarity, we will use vector notation:

$$\vec{A} = \begin{bmatrix} a_0 \\ a_1 \\ - \\ - \\ - \\ a_n \\ 2\text{-}1 \end{bmatrix}$$

with a_i = Prob (input vector A_i).

The strategy for deciding the "health" of the device under test is simply to compare the number of ones counted during the second step of the experiment with the correct number for every output line. If the random number generator is reset at the beginning of each test experiment, it will always produce the same sequence of test vectors. This allows exact comparison. Any discrepency between the observed statistic and the correct one indicates the presence of a fault or an improper synchronization. If the random number generator is not reset, then it is not possible to guarantee that two identical circuits produce exactly the same number of ones on each of their outputs (because of the different test sequences). However, as it will be seen later, two

identical circuits, whatever their initial state, will still produce about the same number of ones. So, the criteria for a circuit to pass the test is that, for every output line Z_i, the observed frequency of logic ones, $\hat{z}_i$, does not differ more than ε_i from the correct value z_i.

$$\text{Circuit passes tests} \quad \text{iff} \quad \left\| \hat{z}_i - z_i \right\| < \varepsilon_i$$

The vector $\hat{\vec{z}}$ of the output probabilities $\hat{z}_i$ is called the signature of the circuit under test while the vector $\vec{z}$ of the correct output probabilities z_i is called the correct signature (or reference signature).

III. SYNCHRONIZATION

One of the problems in testing sequential circuits is synchronization. When exercized, the responses of sequential machines are dependent upon their initial states. Deterministic test set generation methods use synchronizing sequences (or homing sequences) to preset the circuit under test in a known state (or to determine the initial state) [R. Boute, 1972]. Compact testing uses a similar approach. A long series of T_o random inputs is injected to the circuit to achieve a probabilistic synchronization.

Let the vector $_t\vec{S}$, called Probabilistic State, denote the state probabilities for the machine after the tth input has been applied.

$$ {}^t\vec{S} = \begin{bmatrix} {}^tS_1 \\ {}^tS_2 \\ - \\ - \\ - \\ {}^tS_q \end{bmatrix} $$

with $_tS_i$ = probability to be in state Q_i after the tth input. From the state transition diagram of the machine and the input probability vector, $\vec{A}$, it is easy to obtain the state transition probability matrix, N:

$$ N = \left[n_{ij} \right]_q^q $$

with n_{ij} = Prob (to go from state Q_i to state Q_j in one step | the input vector is random with probability distribution given by the vector $\vec{A}$).

With such a notation, the probabilistic state after the tth input, $\vec{S}_t$, is

$$\vec{S}_t = \vec{S}_0 \cdot N^t$$

where $\vec{S}_0$ is the probabilistic state at the start of the test.

If the machine under test is strongly connected (which is to say that from every state it is possible to reach any other state), then the matrix N corresponds to the matrix of an ergodic Markov chain [T.L. Booth, 1967]. Thus, the probabilistic state, $\vec{S}_t$, approaches a constant value, $\vec{w}$, as the length of test, t, increases:

$$\lim_{t \to \infty} \vec{S}_t = \lim_{t \to \infty} \left[\vec{S}_0 \cdot N^t \right] = \vec{w}.$$

This means that after a long sequence of random inputs, the probability of any given state is fixed and independent of the initial state. So, one can say that any long sequence of random inputs is a probabilistic synchronizing sequence in the sense that the final probabilistic state is independent of the initial state.

The necessary number of random input needed to achieve proper probabilistic synchronization ($\vec{S}_t$ is different from $\vec{w}$ by less than $\vec{\varepsilon}$) is directly dependent upon the eigenvalues of the matrix N. Any power of the matrix N can be written as

$$N^t = \sum_{i=1}^{q} \lambda_i^t \cdot N_i$$

where the λ_i's are the eigenvalues of N and the N_i's matrices are

independent of t. The convergence radius of $\vec{S}_t$ (towards $\vec{w}$) is the eigenvalue with the larger absolute value (besides the eigenvalue, $\lambda_1=1$, which always exists). For example, a binary counter with u stages (counting from 0 to $2^u - 1$) will reach its probabilisticly synchronized state $\vec{w}$, within a precision of 10^{-X}, after a sequence of approximately $.46 \times X \times 2^{2u}$ random inputs of the same likelihood. In this example, the required length of the synchronizing sequence is fairly large (around 1.3 million inputs for a 10-stage counter to reach the steady state within .1%). However, this is a worst case example and, even though, the time required for such a probabilistic synchronizing sequence will be less than 1 second for most present-day implementations.

When the random number generator is reset at the beginning of each new test experiment, deterministic synchronization can be achieved if the sequence of T_o random inputs contains a subsequence which is a deterministic synchronizing sequence. However, if the length of the deterministic synchronizing sequence is substantial, the likelihood that it will occur in a random sequence may be extremely small. For example, if the shortest synchronizing is 100 inputs long and the machine has 10 input variables, it may require as many as 10^{300} random inputs of the same likelihood to have a significant chance to achieve deterministic synchronization (cf., Appendix I). So, unless synchronizing sequences are quite short (for example, when there are reset lines), it is unlikely that sequential machines are deterministicly synchronized at the beginning of the statistic gathering (cf, Figure 2).

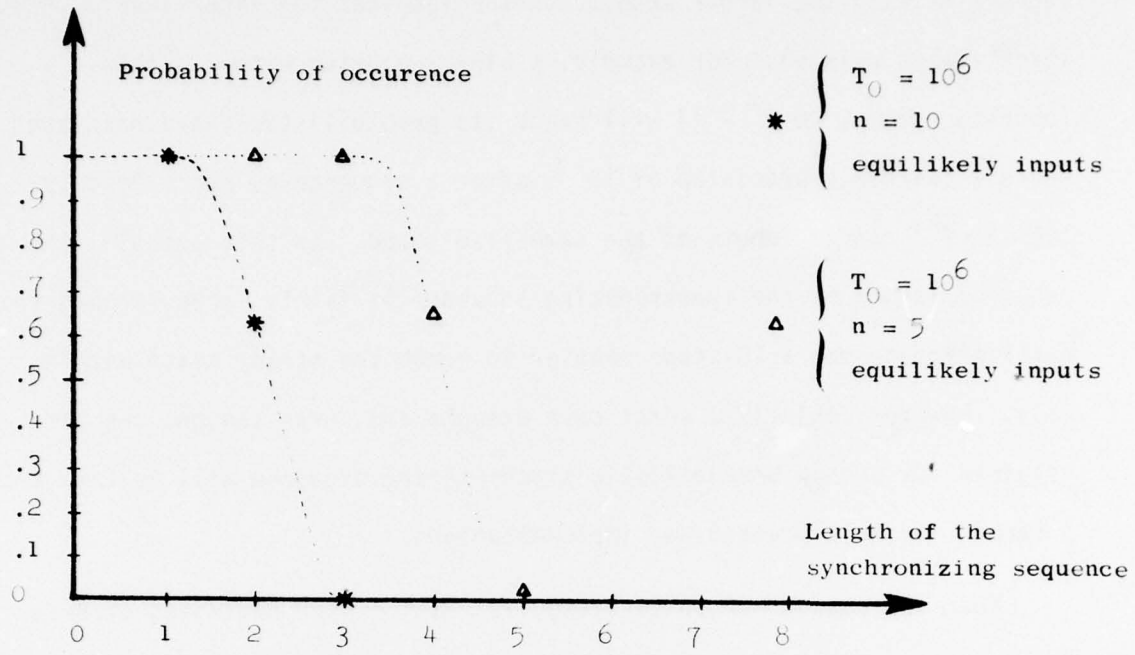


Fig. 2. Probability that a random sequence contains a synchronizing sequence.

IV. REJECTION OF FAULT-FREE CIRCUITS

Some fault-free circuits may not pass the test because of the randomness of the test sequence and its finite length. In the following, we will assume that the internal states constitute the outputs (one line for each state). So, the signature of the circuit under test, $\hat{\vec{z}}$, is

$$\hat{\vec{z}} = \frac{1}{T} \sum_{t=1}^{T} {}_{T_o+t}\vec{S} \cdot N^t = \frac{1}{T} \left[{}_{o}\vec{S} \cdot \sum_{t=1}^{T} N^{T_o+t} \right]$$

As it can easily be seen, the signature of the circuit under test approximates $\vec{w}$, which is the correct signature. The matrix N can be written as :

$$N = \sum_{i=1}^{q} \lambda_i \cdot N_i$$

(orthogonal decomposition, $\lambda_i = 1$, the λ_i ordered by decreasing magnitude)

and

$$N^t = \sum_{i=1}^{q} \lambda_i{}^t \cdot N_i$$

So, the difference between $\hat{\vec{z}}$ and $\vec{w}$ is

$$\hat{\vec{z}} - \vec{w} = \frac{1}{T} \left[{}_{o}\vec{S} \cdot \sum_{t=1}^{T} \left(\sum_{i=2}^{q} \lambda_i{}^{T_o+t} \cdot N_i \right) \right]$$

As T_o is fairly large, one has only to consider the terms in λ_2 (λ_1 being 1 is cancelled by $\vec{w}$). So,

$$\left\| \hat{\vec{z}} - \vec{w} \right\| \simeq \frac{1}{T} \cdot \left\| \frac{\lambda_2{}^{T_o+1}}{1-\lambda_2} \right\| \cdot {}_{o}\vec{S} \cdot N_2$$

$$\left\| \vec{\hat{z}} - \vec{w} \right\| \simeq \left[\frac{1}{T} \cdot \frac{\lambda_2}{1-\lambda_2} \right] \cdot \left[\lambda_2^{T_o} \cdot {}_o\vec{S} \cdot N_2 \right]$$

The second factor represents the accuracy with which the probabilistic synchronization has been achieved. As it is clear from the first term, the probability of rejecting fault free units is extremely low (even when probabilistic synchronization was poorly achieved) if the eigenvalue with higher absolute value, λ_2, is negative. Figure 3 gives the dependency between the approximation of $\vec{w}$ by $\vec{\hat{z}}$ and the length of the test.

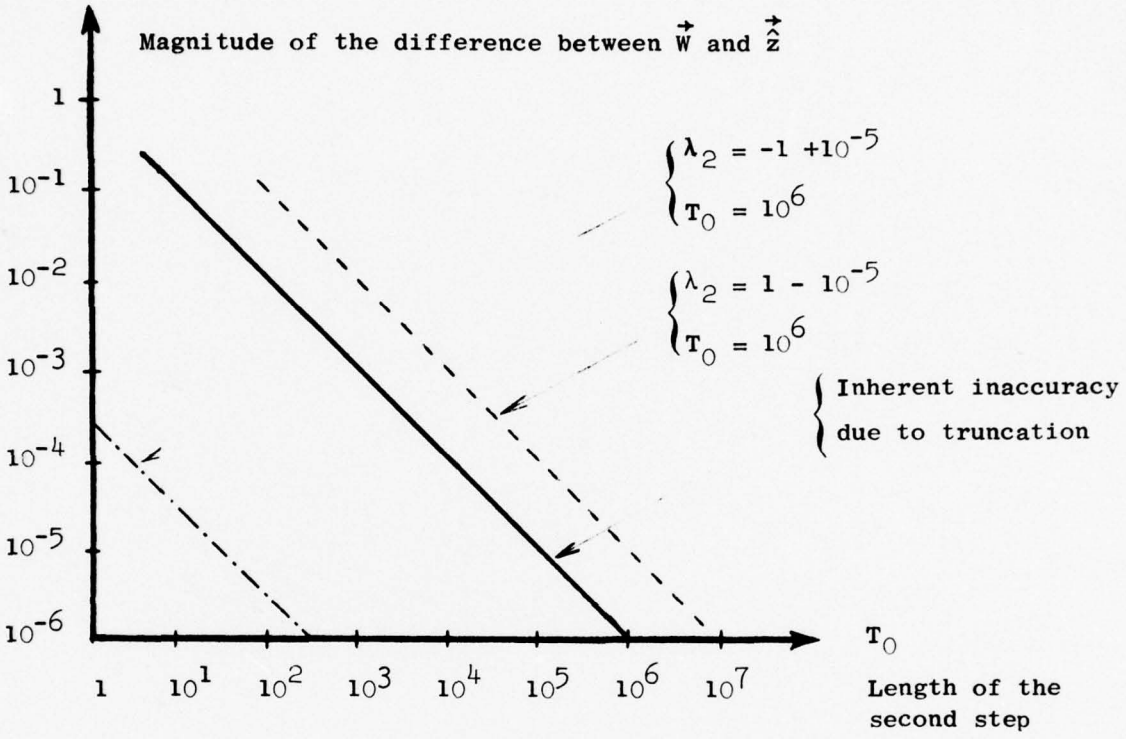


Fig. 3. Difference between the steady state W and its approximation $\hat{\vec{z}}$ as a function of the test length.

V. DETECTION OF FAILURES

V.1 INHERENT LIMITATIONS OF COMPACT TESTING

It has been shown by [E.J. McCluskey, 1975] that random testing can detect any failure inside a combinational circuit, if the input probabilities are correctly chosen. The output probability becomes the fixed point decimal representation of the truth table (expressed as a binary number). So, random testing can be used to identify combinational circuits (even though it is highly impractical). However, for sequential circuits such a statement is false. Whatever the input probabilities, whatever the sequential machine under test, there will always be different machines which have the same signature (so they will pass the test). The proof is fairly simple. The signature, $\vec{w}$, of a sequential machine is given by the following equation:

$$\vec{w} \cdot M = \vec{W}$$

But any matrix M' obtained from M by some column permutation will have the same signature. So, compact testing cannot guarantee that it will detect all the possible failures (and this is independent of the test length). However, most of the failures that do occur can be detected.

V.2 FAILURES IN THE OUTPUT CIRCUITRY

Most of the sequential machines have the architecture of Figure 4. The memory elements are flip flops. They are controlled by a combinational circuit synthetizing the exitation functions from the circuit inputs and the flip-flop outputs. The circuit outputs are obtained by combinational logic. Failures can occur either in the memory elements (flip flops),

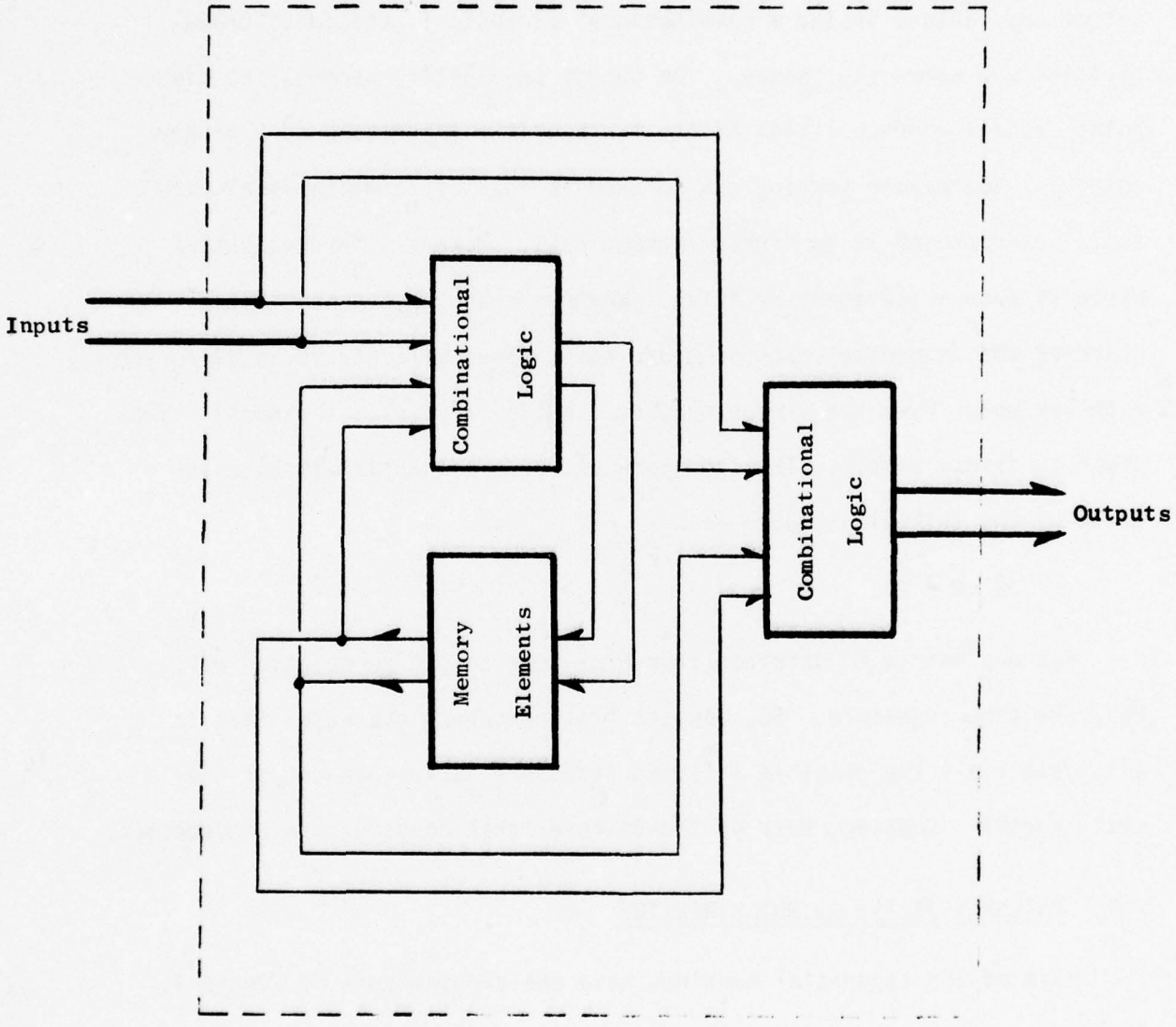


Fig. 4. General architecture of sequential circuits.

in the combinational circuit controlling these flip-flops or in the combinational logic synthetizing the circuit outputs. For simplicity of this study, we will consider these three cases separately. It is quite intuitive that, in general, multiple failures are easier to detect (cumulative effects).

The failures that are restricted to the combinational logic synthetizing the circuit outputs from the inputs and the flip-flop outputs (Mealy-type machines) do not affect the state transitions. So, this problem is analogous to the problem of detecting failures in combinational logic (with input probabilities determined by the circuit probabilistic state).

Failures can affect the validity of one or several of the output variables. It is obvious that the failures that affect several output lines are easier to be detected (the probabilities of ones on several output lines will not match the correct values). So, one can get a lower bound for detection efficiency by looking only at single output circuits. The output, Z, is a combinational function of the inputs (A_i's) and the states (Q_j's). When the circuit is fault-free, the output probability is z. The possible faults that affect the output circuitry may be very varied in terms of their effects. A stuck-at fault directly on the output line will be immediately detected (the probability, $\hat{z}$, of the faulty circuit will always be 0 or 1). In general, one can get a very conservative model for the faults if one considers that on the average a fault will affect only a few cells of the truth table (output as a combinational function of the inputs and states). It is analogous to say that the output will be valid most of the time but incorrect for a few combinations of input variables and internal states.

Under this assumption, it has been shown by [J. Losq, 1976] that the distribution of the output probability, $\hat{z}$, over all possible faulty circuits is a gaussian distribution.

$$\text{Prob}\left(\hat{z} \in \left[u - \frac{du}{2},\ u + \frac{du}{2}\right]\right) = \text{Gauss}\ (u,\ z + \Delta,\ \sigma^2)\ .\ du$$

with z = output probability of the correct circuit,

$\Delta = (1-2z) \cdot y$,

y = proportion of the cells in the truth table that are affected by a fault (characterizes the extend of a failure),

σ^2 = variance $= y(1-y) \cdot \left(\vec{A}^{tr} \cdot \vec{A}\right) \cdot \left(\vec{w} \cdot \vec{w}^{tr}\right)$.

The fact that the distribution is not centered around the correct probability and that the variance is quite small implies that most of the failures in output circuitry will be detected, cf. Figure 5 (the difference between $\hat{z}$ and z is very likely to be greater than the acceptance window ε). So, one can state that compact testing is efficient to detect failures located in the combinational logic synthesizing the outputs. For example, in the case of Figure 5, more than 99% of all failures will be detected.

V.3 FAILURES IN THE MEMORY ELEMENTS

The simplest and most general assumption to make concerning failures in the memory elements (flip-flops) is that they will correspond to one of the flip-flops being stuck (stuck-at failure at the flip-flop output). When the output of a flip-flop is stuck, half the states are unreachable. Half the columns and rows of the transition matrix N' will be zero.

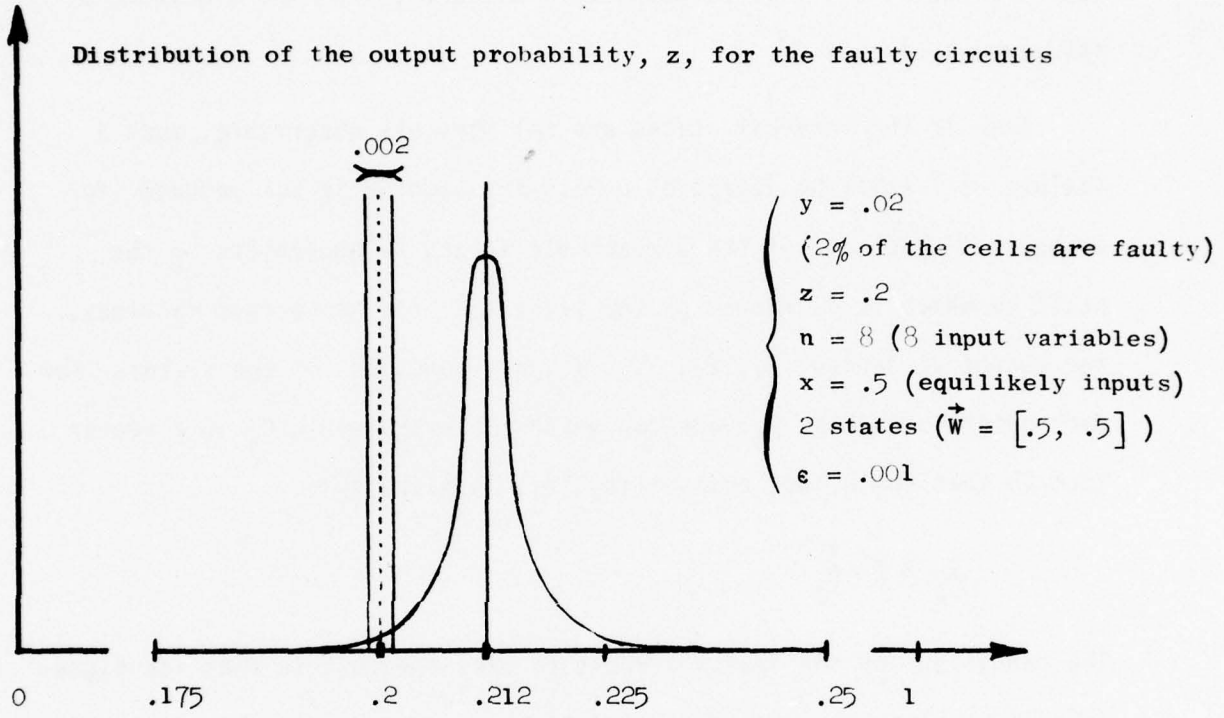


Fig. 5. Distribution of the output probability, $\hat{z}$, for the faulty circuits (the test acceptance window is shown for comparison).

Consequently, half of the elements of the steady-state vector $\vec{w}'$ are also zero. If the internal states are directly observable at the the circuit output, these failures will be immediately detected. The signature of the faulty circuit, $\vec{w}'$, will be completely different from the signature of the correct circuit, $\vec{w}$.

Even if the internal states are not directly observable, such a failure will still be detected, unless the machine is not reduced (for example, if each one of the unreachable states is equivalent to the state to which it is mapped by the failure). For Moore-type machines, the output variables, $Z_1, Z_2, \ldots, Z_m$, are functions of the states. For each output variable, Z_j, one can write the truth table C_i in a vector form so that the output probability, z_j, is given by:

$$z_j = \vec{w} \cdot \vec{C}_j$$

The condition for the faulty circuit to pass the test is that its signature is equal to the reference signature:

$$\vec{w}' \cdot \vec{C}_j = \vec{w} \cdot \vec{C}_j \qquad \forall j \in \{1, 2, \ldots, m\}$$

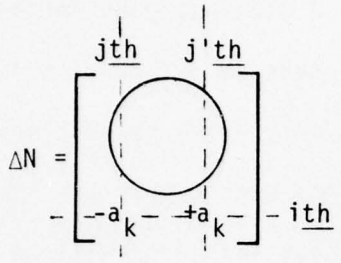
But every element of $\vec{w}'$ is different from the corresponding element in $\vec{w}$ (half of $\vec{w}'$ is zero). So, this set of m equations is extremely restrictive on the values of $\vec{w}'$ that satisfy it. So, one can say, without loss of generality, that the signature of the faulty circuit will differ from the reference signature. Mealy-type machines can be treated similarly. So, as a general statement, it is safe to say to every failure that affects the memory elements will be detected by compact testing.

V.4 FAILURES IN THE COMBINATIONAL LOGIC CONTROLLING THE MEMORY ELEMENTS

Failures that take place in the combinational logic that synthetizes the exitations for the flip-flops affect the state transition diagram of the circuits. Failures are quite diverse. A stuck-at constant value on the R input of an R-S flip-flop may be analogous to a flip-flop failure. On the other hand, some failures may change only a few transitions in the transition diagram (for example, a failure may change only the transition between states Q_i to Q_j under input A_k). These last ones will be the most difficult to detect because their effects on the system operation is somewhat limited (in a statistical sense). So, as it was done for the output combinational logic, we will only consider these failures in the analysis. This will provide a meaningful lower bound for detection efficiency.

Each of the flip-flops that compose the circuit memory has its own exitation synthetized by combinational logic. It is natural to assume that failures will affect the exitation of only one flip-flop. It is also natural to use the same model as used in Section V.2 to describe the effects of falures. Each failure changes only a few cells in the exitation truth table (table giving the flip-flop exitation as a function of the circuit inputs and internal states). The cells affected are randomly distributed all over the truth table. For every faulty cell, the corresponding state transition (inputs + state → exitation → state transition) will be different from the correct one. Reciprocally, for every correct cell in the exitation table both the faulty and the fault-free machines have the same transition.

If the cell corresponding to input A_k and state Q_i is faulty, then the normal transition from state Q_i to state Q_j under input A_k is replaced by a transition to state $Q_{j'}$. The corresponding change, ΔN, in the transition matrix N, is



The new next state $Q_{j'}$ is dependent of Q_j. If Q_j corresponds to 000...00 in the flip-flops and if the failure affects the first flip-flop, then Q_j corresponds to 100...00.

The corresponding change in $\vec{w}$, $\Delta\vec{w}$, is expressed as:

$$\Delta\vec{w} \cdot (I - N - \Delta N) = \vec{w} \cdot \Delta N$$

If $\vec{w} = [w_1, w_2, \ldots, w_q]$

then $\Delta\vec{w} \cdot (I - N - \Delta N) = [0,0,\ldots,0,-a_k \cdot w_y,0,\ldots,0,a_k\ w_j,\ 0,\ldots 0]$

So, there will always be a change in $\vec{w}$, $\Delta\vec{w}$, associated with such a failure. This change, $\Delta\vec{w}$, is the basic reason why compact testing can detect these failures.

In general, failures in the logic synthesizing the exitation functions will invalidate several cells of the exitation truth table. The change in $\vec{w}$ associated with each faulty cell is given by the previous equation. It can be easily seen that the effects of several faulty cells is cumulative:

$$\Delta\vec{w}\ (I - N - \Delta N) = \Delta\vec{w}\ (I - N) - \Delta\vec{w} \cdot \Delta N \simeq \Delta\vec{w}\ (I - N)$$

So, if the changes on N, associated with the v faulty cells are respectively ΔN_1, ΔN_2, ..., ΔN_v, then

$$\Delta\vec{w}\ \ (I - N) \simeq \sum_{i=1}^{v} \vec{w} \cdot \Delta N_i = \vec{w} \sum_{i=1}^{v} \Delta N_i \quad .$$

If the number of faulty cells is small (compared to the total number of cells in the truth table), then one can state that at least two elements of $\vec{w}$ will be changed by the faults. The average magnitude of this change is

$$\Delta w \simeq w \cdot \sum_{i=0}^{2^n-1} a_i^{\,2} = w \cdot \prod_{i=1}^{n} \left[x_i^{\,2} + (1 - x_i)^2 \right]$$

So, the relative change is directly dependent upon the input probabilities x_i (the characteristics of the random number generator). It can be noted that the variation in w is independent of the function realized by the circuit. One can also note that there is a trade-off for choosing the set of input probabilities (the x_i's). Detection of failures in the output circuitry are facilitated when the x_i's are close to .5(this decreases the variance, σ^2, in the distribution of the signature, cf. Section V.2). On the other hand, detection of failures in the exitation circuitry is improved if the x_i's are far from .5.

So, most of the failures located in the exitation circuitry can be detected by compact testing. If they affect very significantly one exitation function, then they tend to have effects similar to memory

failures, and thus, they will be easily detected. Even when their effects are very limited, they will produce a change in the steady-state of the circuit. Such a change can be detected if the test is long enough. Figure 6 gives the minimum test length required to detect one of these very subtle failures. It should also be noted that clock-related failures will be detected by compact testing for they will be equivalent to memory failures or exitation failures.

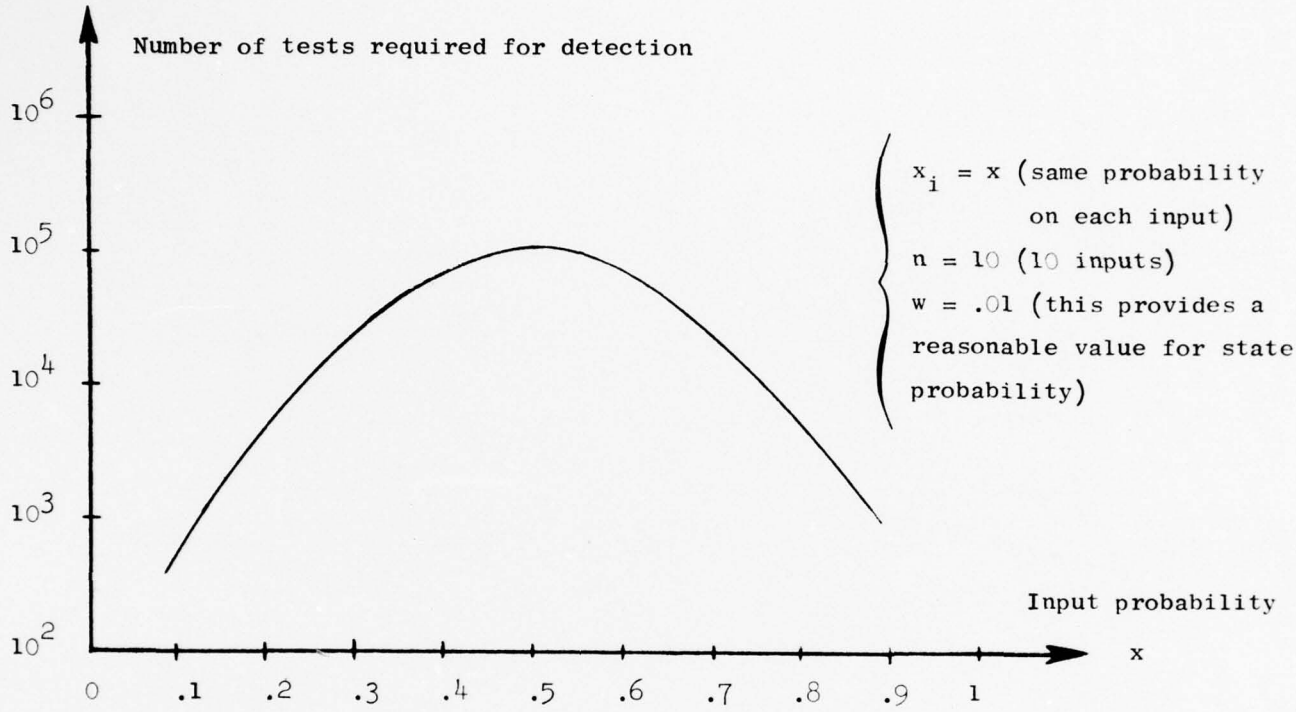


Fig. 6. Minimum number of test inputs to achieve detection of failures in the logic synthesizing the flip-flops exitations.

VI. CONCLUSIONS

Compact testing is a very simple method to test complicated circuitry. Circuit analysis is avoided. Testing equipment is extremely simple and can be used with almost any kind of circuit. There is no need for large libraries of test sets or reference output sequences. This is obtained at the cost of far longer test sets. However, the speed of most digital circuits nowadays allows several million inputs per second. So, very large test sets (10^6 inputs and higher) are not a penalty, especially when they are random (algorithmic generation).

It has been previously shown that random testing is an efficient method to test combinational circuits. However, the problems associated with sequential machines can make one doubt its usefulness for sequential machines (even though it is practically used for this purpose). Here, we showed that the problem of initial state can be simply overcome. A long sequence of random inputs, during which one does not look at the circuit outputs, acts as a synchronizing sequence for compact testing, even when the machine does not possess deterministic synchronizing sequences. The probability that compact testing rejects fault-free circuits can be made arbitrarily small by increasing the length of the synchronization period. For most practical applications, the rate of rejecting falut-free circuits is negligible.

Even though compact testing can never guarantee one hundred percent confidence in its results, it is still an efficient way to detect most of the failures that can occur in sequential machines. Failures affecting

the memory elements (or the delay elements in the feedback loops) are guaranteed to be detected. Similarly, permanent clock failures do not escape detection. Failures in the combinational logic synthesizing the output functions from the circuit inputs and its states, are also likely to be detected. It was shown that the corresponding signature differs from the correct one by a quantity that is a random variable of non-zero mean and extremely small variance. so, the efficiency to detect these failures is a monotonically increasing function of the test length. Most of the failures that affect the exitation of the flip-flops (or the state transitions) can also be detected. Depending on the extent with which they affect the operation of the circuit, the change they induce on the circuit signature is more or less accentuated. Failures that drastically change the circuit operation are extremely likely to be detected. However, even the more subtle failures, those which change only one state transition, can be caught by the test if it is long enough.

Because of the similarity between compact testing and random test set generation, one may hope that the efficiency of compact testing could be enhanced by some kind of interactive use (or feedback between the circuit signature and the random number generation). Investigation of this problem may lead to a very general and efficient way to test very large digital systems.

APPENDIX I

Probability that a random sequence of length T contains a given subsequence of length ℓ.

This is a well known problem whose general solution is extremely complex. However, for our purposes, one can get a simple approximation. Let us assume: all the letters of the alphabet (all possible inputs) have the same likelihood (with probability $a = 2^{-n}$) and the given subsequence does repeat the same letter (each letter appears at most once).

Even though this seems to be a strong assumption, it gives a good approximation.

With these assumptions, we can model the process as a Markov chain. The state, S_i (i from o to ℓ) indicates that, while the random sequence is drawn, the last i letters correspond to the first ith letters of the subsequence. The probability transition matrix, M, for this Markov chain is

$$M = \begin{bmatrix} 1-a, & a, & o, & \ldots, & o \\ 1-a, & o, & a, & \ldots, & o \\ 1-a, & o, & o, & \ldots, & a \\ o, & o, & o, & \ldots, & 1 \end{bmatrix}$$

The characteristic polynomial is $(\lambda-1)\dfrac{\lambda^{\ell+1} - \lambda^{\ell} - a^{\ell+1} + a^{\ell}}{\lambda - a}$.

One of the eigenvalue is 1 and the one with the next higher absolute value is closely approximated by $1 - (1-a)a^{\ell}$. So the convergence radius is $1 - (1-a)\ a^{\ell}$. So,

Prob (to be in state S_ℓ after T inputs) = Prob (the random sequence contains the given subsequence)

$$\simeq 1 - \text{Exp}\ (-(1-a)\ \ a^{\ell}\ T)\ .$$

VI. REFERENCES

[Agrawal, P., et al., 1972] Agrawal, P. and V.D. Agrawal. "Probabilistic Analysis of Random Test Generation Method for Irredundant Combinational Logic Networks," IEEE Trans. on Computers, Vol. C-24, pp. 691-695, July 1975.

[Agrawal, V.D., et al., 1972] Agrawal, V.D. and P. Agrawal, "An Automatic Test Generation System for ILLIAC IV Logic Boards," IEEE Trans. on Computers, Vol. C-21, pp. 1015-1017, September 1972.

[Arbid, M.A., 1969] Arbid, M.A., Theories of Abstract Automata, Prentice-Hall, 1969.

[Booth, T.L., 1967] Booth, T.L., Sequential Machines and Automata Theory, J. Wiley & Sons, New York, 1967.

[Bouricius, W.G., et al., 1971] Bouricius, W.G., E.P. Hsieh, G.R. Putzolu, J.P. Roth, P.R. Schneider and C.J. Tan, "Algorithms for Detection of Faults in Logic Circuits," IEEE Trans. on Computers, Vol. C-20, pp. 1258-1264, November 1971.

[Boute, R., 1972] Boute, R., "Algebraic Properties of Test Sequences and Fault Relations," Tech. Rpt. No. 37, Digital Systems Laboratory, Stanford University, Stanford, California, November 1972.

[Breuer, M.A., 1971] Breuer, M.A., "A Random and an Algorithmic Technique for Fault Detection Test Generation for Sequential Circuits," IEEE Trans. on Computers, Vol. C-20, pp. 1364-1370, November 1971.

[Hayes, J.P., 1975] Hayes, J.P., "Testing Logic Circuits by Transitions Counting," Proc. Fifth Int'l Symposium on Fault-Tolerant Computing, pp. 215-219, Paris, June 1975.

[Hayes, J.P., 1976] Hayes, J.P., "Check Sum Test Methods," Proc. Sixth Int'l Symposium on Fault-Tolerant Computing, pp. 114-120, Pittsburg, June 1976.

[Hayes, J.P., 1976] Hayes, J.P., "Transition Count Testing of Combinational Logic Circuits," IEEE Trans. on Computers, Vo.-25, pp. 613-620, June 1976.

[Losq, J., 1976] Los, J., "Referenceless Random Testing," Proc. Sixth Int'l Symposium on Fault-Tolerant Computing, pp. 108-113, Pittsburg, June 1976.

[McCluskey, E.J., 1965] McCluskey, E.J., Introduction to the Theory of Switching Circuits, McGraw-Hill, New York, 1965.

[McCluskey, E.J., et al., 1975] McCluskey, E.J. and K.P. Parker, "Boolean Networks Probabilities and Network Design," Tech. Note No. 60, Digital Systems Laboratory, Stanford University, Stanford, California, July 1975.

[Parker, K.P., 1976] Parker, K.P., "Compact Testing: Testing with Compressed Data," Proc. Sixth Int'l Symposium on Fault-Tolerant Computing, pp. 93-98, Pittsburg, June 1976.

[Parker, K.P., 1976] Parker, K.P., "Probabilistic Test Generation," Ph.D. Thesis, Digital Systems Laboratory, Stanford University, Stanford, California, May 1976.

[Poage, J.P., et al., 1964] Poage, J.P. and E.J. McCluskey, "Derivation of Optimal Test Sequences for Sequential Machines," Proc. Fifth Annual Symposium on Switching Theory and Logical Design, pp. 121-132, 1964.

[Rault, J.C., 1971] Rault, J.C., "A Graph Theoretical and Probalistic Approach to the Fault Detection of Digital Circuits," Proc. First Int'l Symposium on Fault-Tolerant Computing, IEEE Computer Society Pub. 71C-G.C, pp. 26-29, March 1971.

[Roth, J.P., et al., 1967] Roth, J.P., W.G. Bouricius and P.R. Schneider, "Programmed Algorithms to Compute Tests to Detect and Distinguish between Failures in Logic Circuits," IEEE Trans. on Electronic Computers, Vol. EC-16, pp. 567-580, October 1967.

[Schnurmann, M.D., et al. 1975] Schnurmann, H.D., E. Lindbloom and R.G. Carpenter, "The Weighted Random Test-Pattern Generator," IEEE Trans on Computers, Vol. C-24, pp. 695-700, July 1975.

[Seller, F.F., et al., 1968] Sellers, F.F., M.Y. Hsiao and L.W. Bearnson, "Analyzing Errors with the Boolean Difference," IEEE Trans. on Computers, Vol. C-17, pp. 676-683, July 1968.

[Shedlestky, J.J., 1975] Shedlestky, J.J., "A Rationale for the Random Testing of Combinational Digital Circuits," Proc. CompCon 1975 Fall, pp. 5-8, September 1975.

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Compact testing uses random inputs to test digital circuits. Detection is achieved by comparison between some statistic property of the circuit under test, like the frequency of ones on the output line, and the same property for the fault-free circuit. In this paper we show that compact testing can be used efficiently for sequential machines, although it has some inherent limitations. Synchronization is achieved by a long sequence of random inputs whose length is circuit dependent. However, for most sequential circuits, synchronization can be achieved in a few seconds. The great majority of failures inside the memory elements are easily detected

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20. Abstract (continued)

even with short tests. Compact testing also detects most of the failures in the combinational parts. There, its efficiency is largely dependent upon the test length and also the characteristics of the random number generators. However, even the most subtle failures may be detected if the test has sufficient length. Some of the requirements and trade-offs to achieve efficient detection are presented.

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